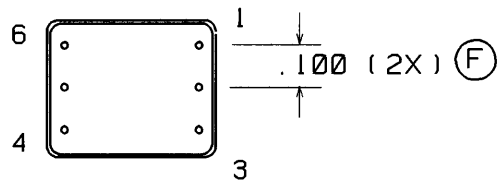
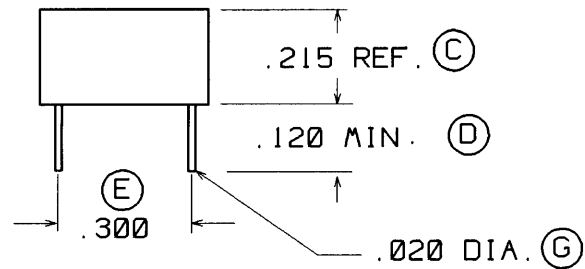
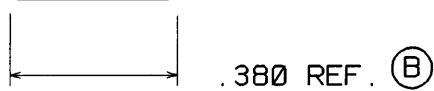
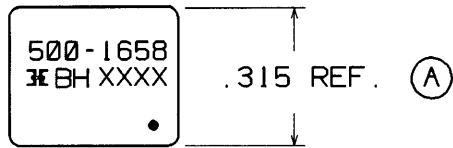
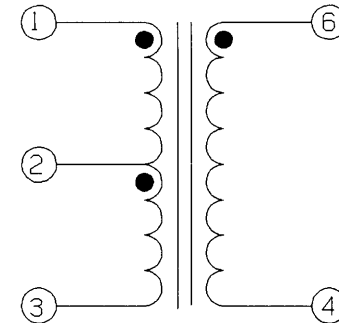


MECHANICAL



SCHEMATIC



ELECTRICAL SPECIFICATIONS


URNS RATIO: 1:1CT

OPEN CIRCUIT INDUCTANCE: 500μH MIN. (1-3)
100 KHz 100mV

DC RESISTANCE: 2 OHMS MAX. (1-3)

ET CONSTANT: 30 Vμ SEC MIN. (BIPOLAR)

HIGH VOLTAGE TEST: 3750 VRMS/1 SEC.

				DESIGNED PER:	 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN ©1998 BH Electronics
E	5-2-00	ECR #4684 CHG. PIN LENGTH	JDC	DRAWN: K. LOFTUS	
D	1-7-00	ADD REFERENCE POINTS	JDC	ENGR. T. GOODRICH	
C	3-26-98	ECR #3723 CHG EPOXY TO COPPS		UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES. TOLERANCES NON-CUMULATIVE.	TITLE
B	4-24-90	REDO SCHEMATIC	JDC		TRANSFORMER
A	9-21-89	CUSTOMER PRINT	TAG	.XX±.01 .XXX±.005	PART NO.
ISSUE	DATE	REVISIONS		SCALE 1:	SHEET 1 / 1
					500-1658