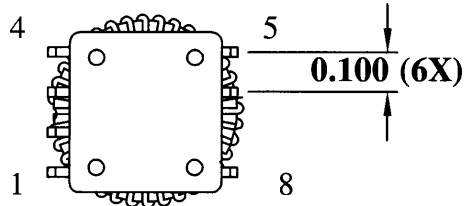
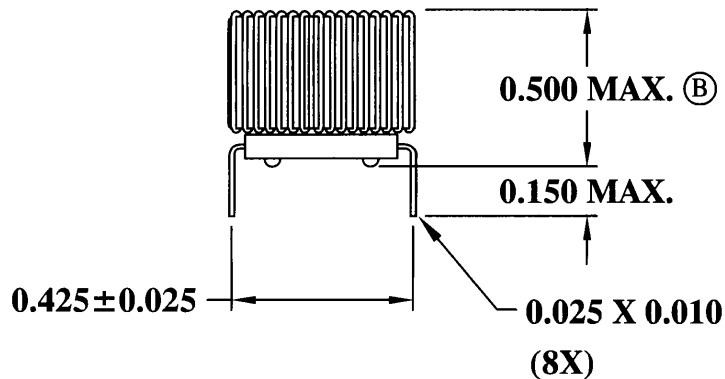
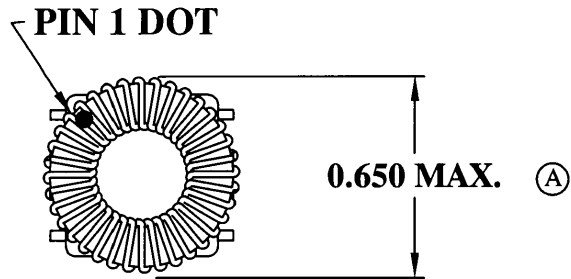
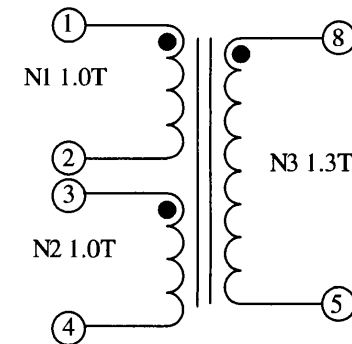


MECHANICAL



SCHEMATIC



ELECTRICAL SPECIFICATIONS

URNS RATIO: 1:1:1.3

OPEN CIRCUIT INDUCTANCE: 1mH MIN. (1-4 SH 2-3) 1 KHz 100mV

PRIMARY LEAKAGE INDUCTANCE: 1.0μH NOM. (1-4 SH 2, 3 SH 5, 8)

INTERWINDING CAPACITANCE: 90pF NOM. (1, 4 - 8, 5 SH 2, 3)


DC RESISTANCE: 0.150 OHMS NOM. (1-4 SH 2, 3)

0.093 OHMS NOM. (8-5)

HIGH VOLTAGE TEST: 2000 VAC / 60 SEC. (1-5 SH 2, 3)

250 VAC / 1 SEC. (1-4)

ET CONSTANT: 100 Vμ SEC. MIN. (BIPOLAR 10 Vp-p) (1-4 SH 2, 3)

ISSUE	DATE	REVISION	BY	DESIGN PER:	 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN © 1998 BH Electronics
F	3-30-05	CORRECT ELECTRICALS	JDC	CATALOG DRAWN: K. LOFTUS ENGR: J. DECRAMER	
E	5-24-04	ADD PIN 1 DOT	JDC		UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES, TOLERANCES NON-CUMULATIVE .XX±.01 .XXX±.005 PAGE 1 OF 1
D	6-24-02	REMOVE PIN 7	JDC		
C	6-13-02	REVISE MECH AND ELECT.			
B	4-25-02	Q10977-1 NOW 500-2582	JDC		
A	4-22-02	CUSTOMER PRINT	JDC		