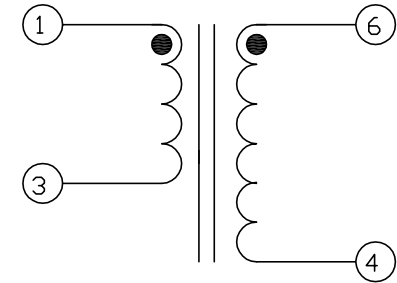
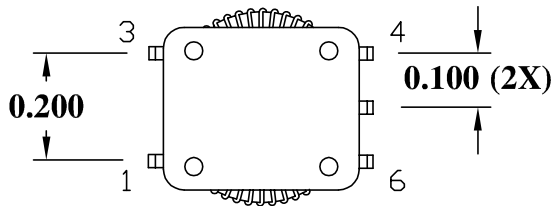
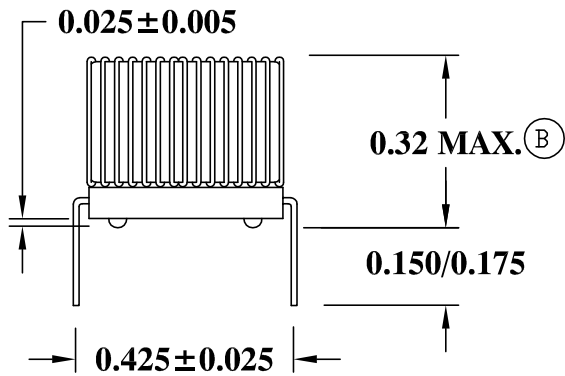
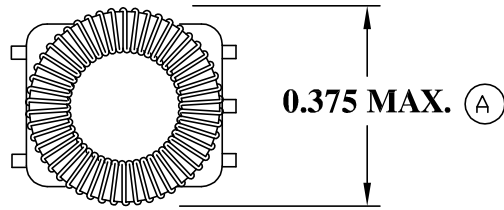


MECHANICAL

SCHEMATIC



ELECTRICAL SPECIFICATIONS

URNS RATIO: 22:28


OPEN CIRCUIT INDUCTANCE: 2.8mH MIN. (1-3) 1 KHz 100mV

PRIMARY LEAKAGE INDUCTANCE: 1µH MAX. (1-3 SH 4-6)

INTERWINDING CAPACITANCE: 41pF NOM.

DC RESISTANCE: 0.70 OHMS NOM. (1-3) 0.90 OHMS NOM. (4-6)

HIGH VOLTAGE TEST: 500 VAC FOR 1 SEC.

				DESIGN PER:		 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN © 1998 BH Electronics	
				BH CATALOG			
F	2-13-12	NOW BH CATALOG	JDC	<input type="checkbox"/> CUSTOM	<input type="checkbox"/> NON-PROPRIETARY		
E	9-24-02	ADD DIM TARGETS	JDC	DRAWN: K. LOFTUS			
D	2-5-98	ECR #3654 UPDATE TO CAD	JDC	ENGR: J. DECRAMER			
C	6-24-93	Q8240 NOW 500-1430	JVM	UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES, TOLERANCES NON-CUMULATIVE .XX±.01 .XXX±.005		TITLE:	
B	6-27-86	REVISE ELECTRICAL	JVM			TRANSFORMER	
A	6-3-86	CUSTOMER PRINT	JVM			PART NO.	500-1430
ISSUE	DATE	REVISION	BY	PAGE 1 OF 1			