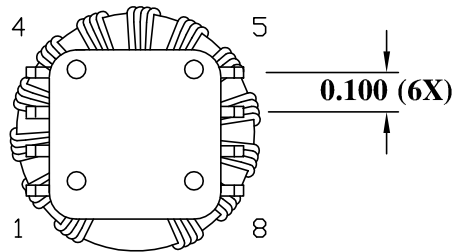
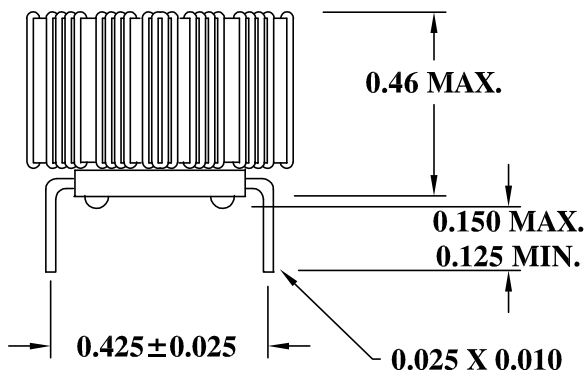
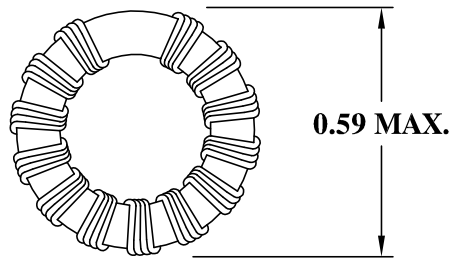
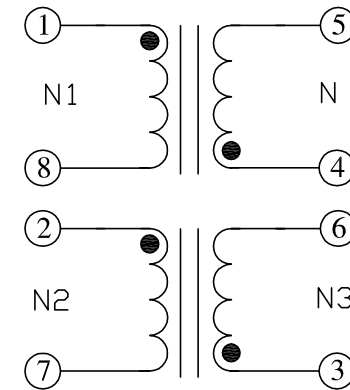


MECHANICAL



SCHEMATIC



ELECTRICAL SPECIFICATIONS


URNS RATIO: 1:1:1

OPEN CIRCUIT INDUCTANCE: 39.75μH - 66.25μH
100 KHz 100mV

INTERWINDING CAPACITANCE: 30pF MAX. (1-2)
120 KHz 50mV

DC RESISTANCE: 0.1 OHMS MAX. (ANY WINDING)

HIGH VOLTAGE TEST: 1000 VDC (WINDING TO WINDING)

G	7-27-07	UPDATE	JDC	DESIGN PER: BH CATALOG	 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN © 1998 BH Electronics
F	12-29-97	CORRECT LOC	JDC		
E	11-14-94	LOC SPEC ±25% NOW TYP.	JDC	<input type="checkbox"/> CUSTOM <input checked="" type="checkbox"/> NON-PROPRIETARY	TITLE: CHOKES COMMON MODE
		ALSO ADD IMPEDANCE		DRAWN: K. LOFTUS	
D	4-21-94	UPDATE TO CADD		ENGR: J. DECRAMER	PART NO. 500-1179
C	7-8-86	REDRAW	JDC	UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES, TOLERANCES NON-CUMULATIVE .XX±.01 .XXX±.005	
B	11-27-85	ADD 1 AND CHG MECH.	JDC		
A	10-3-84	CUSTOMER PRINT	LB		
ISSUE	DATE	REVISION	BY	PAGE 1 OF 1	