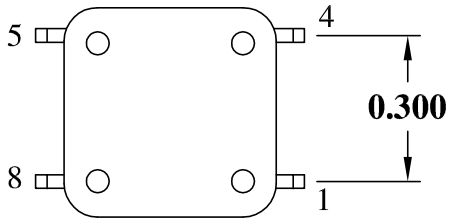
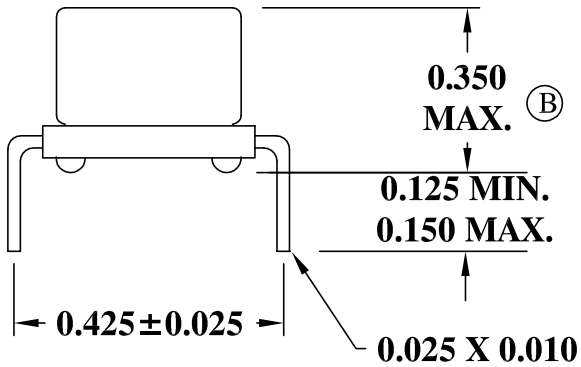
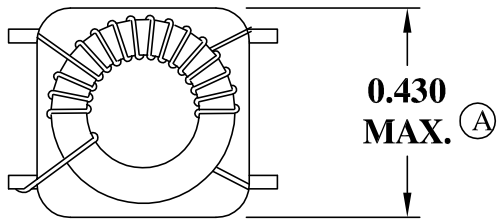
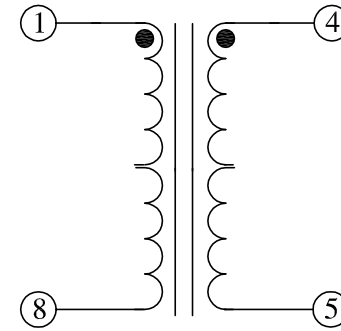


MECHANICAL



SCHEMATIC



ELECTRICAL SPECIFICATIONS

OPEN CIRCUIT INDUCTANCE: 84.4μH NOM. (1-8) (4-5)

READINGS SHOULD BE IDENTICAL

INTERWINDING CAPACITANCE: 20pF MAX.


HIGH VOLTAGE TEST: 1000 VDC (WINDING TO WINDING)

\* IMPEDANCE: 30 OHMS MIN. @ 100 KHz

250 OHMS MIN. @ 1 MHz

2K OHMS MIN. @ 100 MHz

1K OHM MIN. @ 200 MHz

				DESIGN PER:	 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN  © 1998 BH Electronics
G	2-14-12	NON-PROPRIETARY	JDC	<b>BH CATALOG</b>	
F	3-15-08	ADD BH CATALOG	JDC	<input type="checkbox"/> CUSTOM <input checked="" type="checkbox"/> NON-PROPRIETARY	
E	6-16-05	REDUCE Ci SPEC.	JDC	DRAWN: K. LOFTUS	
D	7-7-04	REVISE Ci SPEC.		ENGR: J. DECRAMER	
C	2-26-97	ECR #3176 CUST. P/N & REV.	JDC	UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES, TOLERANCES NON-CUMULATIVE .XX±.01 .XXX±.005	
B	11-25-92	REDO LOC SPEC.		PAGE 1 OF 1	TITLE: <b>COMMON MODE CHOKE</b>
A	8-26-92	CUSTOMER PRINT	JDC		PART NO. <b>500-1910</b>
ISSUE	DATE	REVISION	BY		