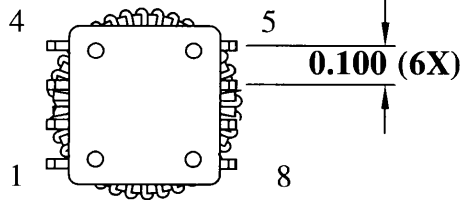
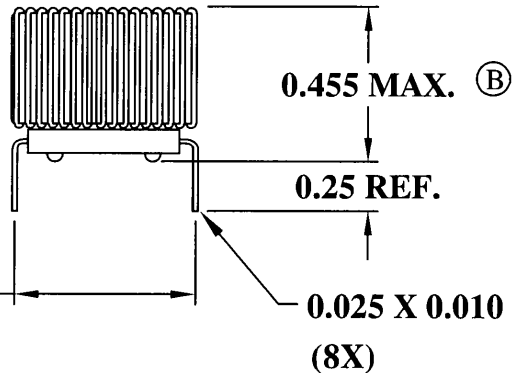
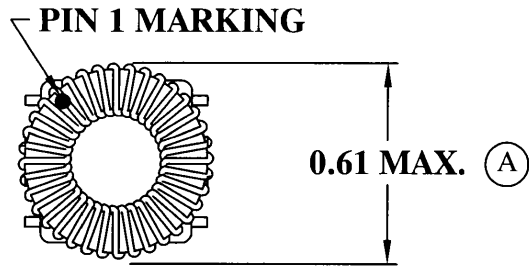
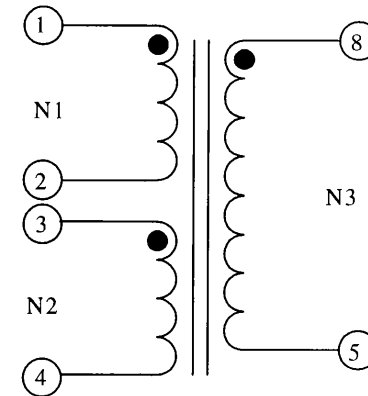


MECHANICAL



SCHEMATIC



ELECTRICAL SPECIFICATIONS

URNS RATIO: 0.5:0.5:1

OPEN CIRCUIT INDUCTANCE: 1mH MIN. (1-4 SH 2, 3)
1 KHz 100mV


PRIMARY LEAKAGE INDUCTANCE: 1.0µH NOM.
(1-4 SH 2, 3 & 8, 5)

INTERWINDING CAPACITANCE: 140pF MAX.
(1-8 SH 1, 2, 3, 4 & 5, 8)

DC RESISTANCE: 0.11 OHMS NOM. (1-2) (3-4)
0.22 OHMS NOM. (8-5)

HIGH VOLTAGE TEST: 2000 VAC / 1 SEC. (1-5) (4-5)

ET CONSTANT: 100 Vµ SEC. MIN. (BIPOLAR 10 Vp-p)
(1-4 SH 2, 3)

				DESIGN PER:	 BH ELECTRONICS, INC. BURNSVILLE & MARSHALL, MN © 1998 BH Electronics
				BH CATALOG	
				CUSTOM <input type="checkbox"/> NON-PROPRIETARY <input checked="" type="checkbox"/>	
				DRAWN: K. LOFTUS	
				ENGR: J. DECRAMER	
E	2-16-06	CORRECT ELECTRICALS	JDC	TITLE: TRANSFORMER	
D	4-29-04	ECR #6091 ADD (4-5) TO HI-POT	JDC		
C	9-17-03	DIM. AND ELECT. CHANGES	JDC	PART NO. 500-2580	
B	4-10-02	CORRECT DIAMETER			
A	3-30-02	CUSTOMER PRINT (Q10977)	JDC		
ISSUE	DATE	REVISION	BY	UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES, TOLERANCES NON-CUMULATIVE .XX±.01 .XXX±.005 PAGE 1 OF 1	